

# Announcements

---

- Office hours today (Wednesday) 2-3pm and tomorrow (Thursday) 1-2pm.
- Please bring all graded homeworks to lab section and show to your TA.

# Triode Region I-V Characteristics

---

$$i_D = K'_n \frac{W}{L} \left( v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS}$$

- When  $v_{DS}$  is small, ignore 2<sup>nd</sup> order terms

$$i_D = K'_n \frac{W}{L} (v_{GS} - V_{TN}) v_{DS}$$

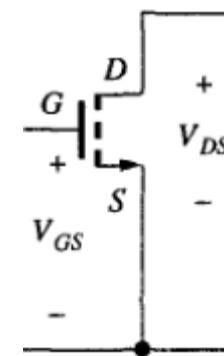
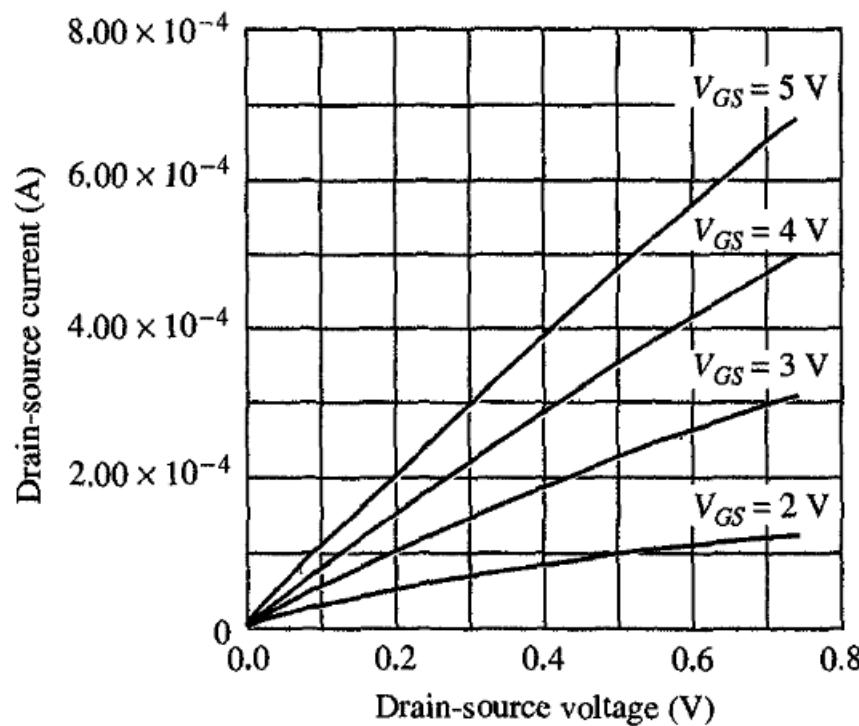
- $i_D$  proportional to  $v_{DS} \Rightarrow$  the MOSFET is like a resistor (resistor value controlled by  $v_{GS}$ )
- On-resistance:

$$R_{on} = \left( \frac{\partial i_D}{\partial v_{DS}} \right)^{-1} = \frac{1}{K'_n \frac{W}{L} (v_{GS} - V_{TN} - v_{DS})}$$

---

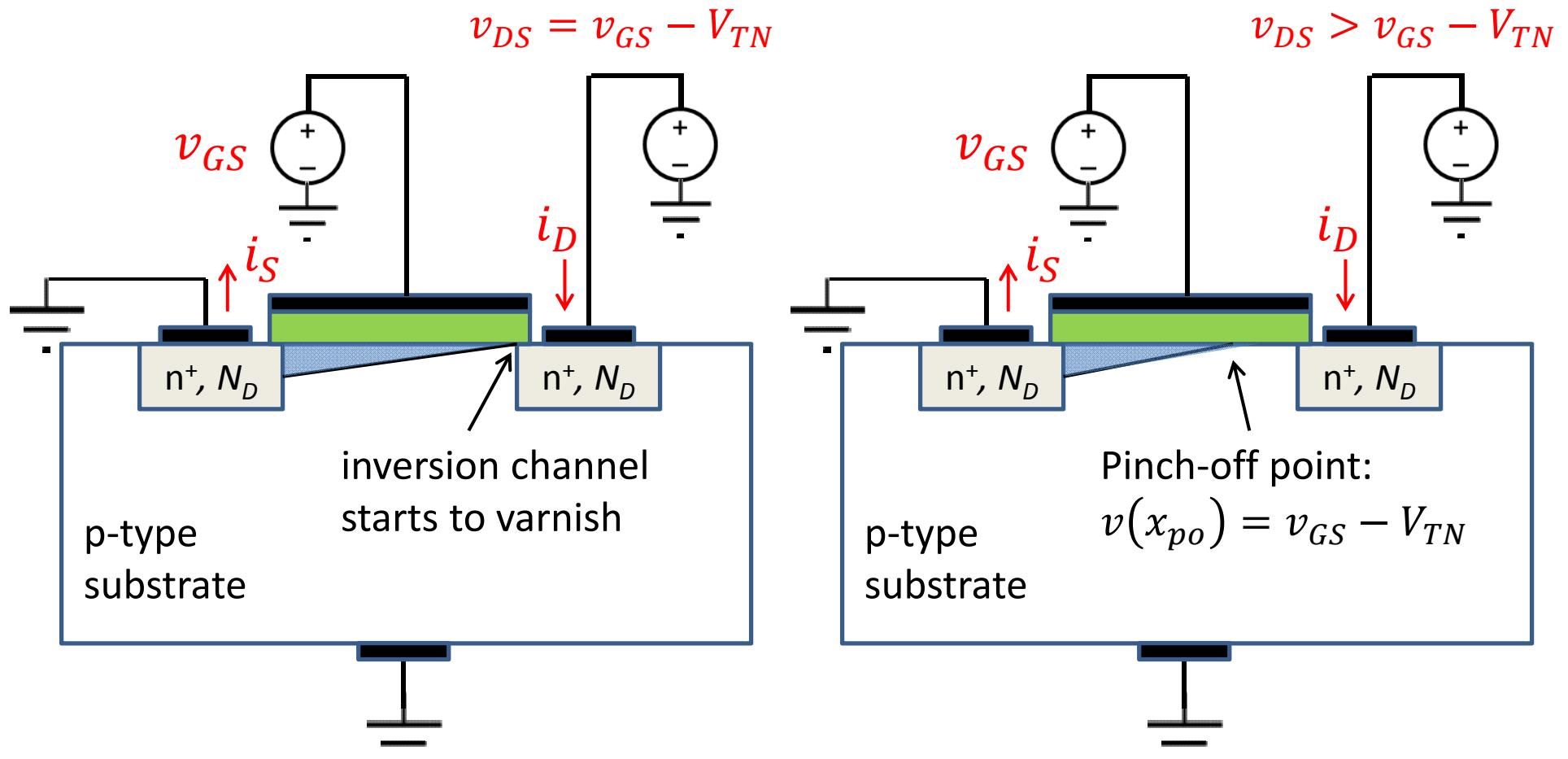
# Triode Region I-V Characteristics

$$i_D = K'_n \frac{W}{L} (v_{GS} - V_{TN}) v_{DS}$$

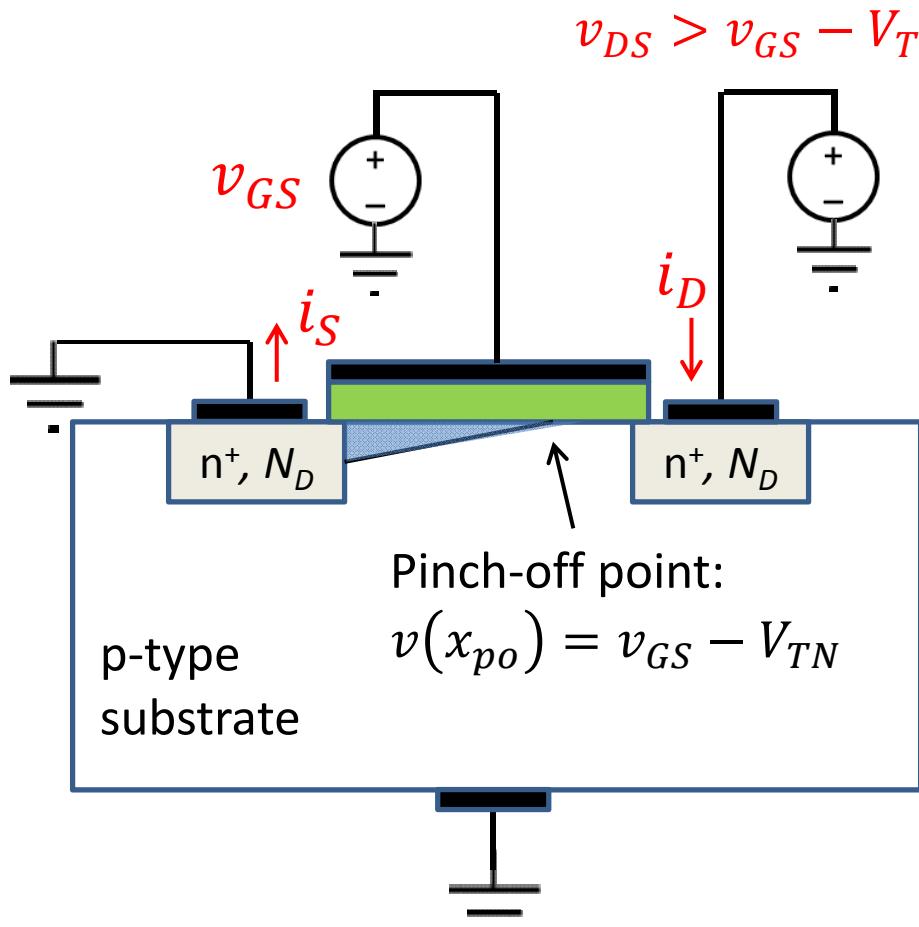


NMOS i-v characteristics in the triode region ( $V_{SB}=0$ )

# Saturation (Pinch-off) region

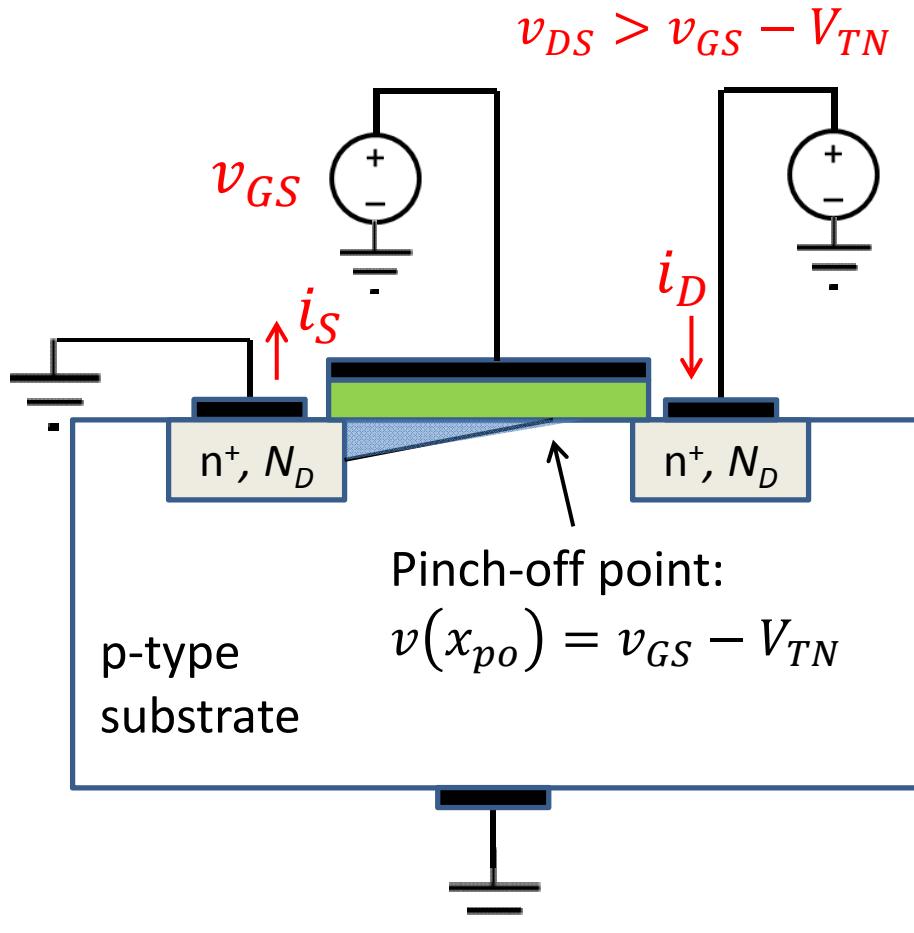


# Saturation (Pinch-off) region



- Onset voltage of saturation is called saturation voltage:  
$$v_{DSAT} = v_{GS} - V_{TN}$$
- Under saturation, voltage across the inversion layer is fixed to be the voltage at the pinch-off point ( $v_{GS} - V_{TN}$ )
- High electric field in the depletion region sweeps the electrons beyond the pinch-off point to the drain.

# Saturation (Pinch-off) region



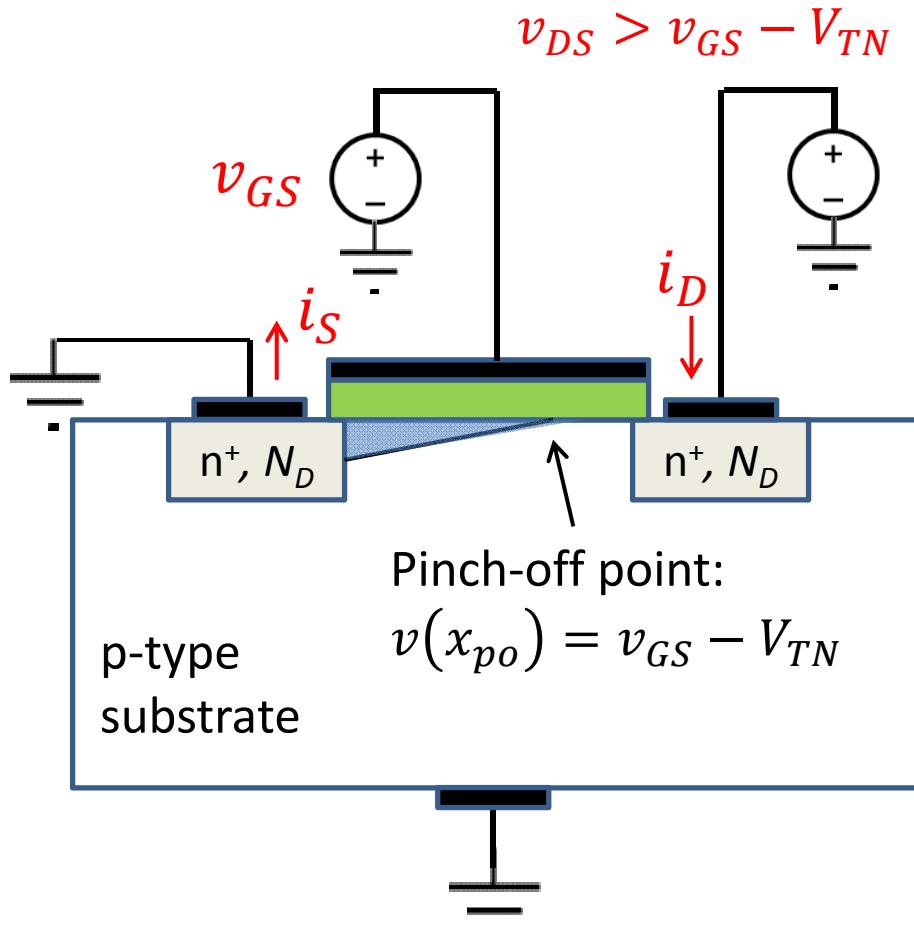
- When  $v_{DS}$  reaches  $v_{DSAT}$ , MOSFET enters the saturation region.
- Further increasing  $v_{DS}$ , voltage across the inversion layer remains constant ( $v_{GS} - V_{TN}$ )
- Thus the saturation region formula is obtained by substituting  $v_{DSAT} = v_{GS} - V_{TN}$  for  $v_{DS}$  in the triode region formula:

$$i_D = \frac{K'_n}{2} \frac{W}{L} (v_{GS} - V_{TN})^2$$

- Saturation condition:

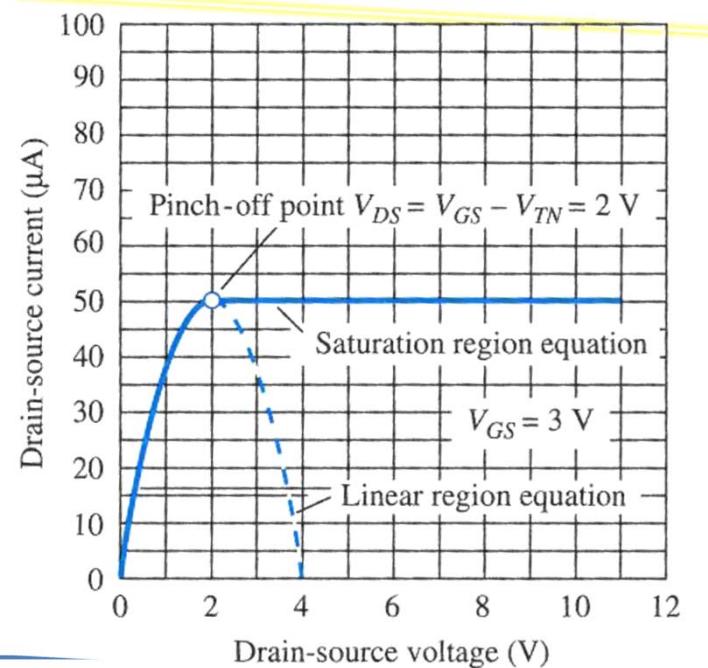
$$v_{DS} \geq v_{GS} - V_{TN}$$

# Saturation (Pinch-off) region

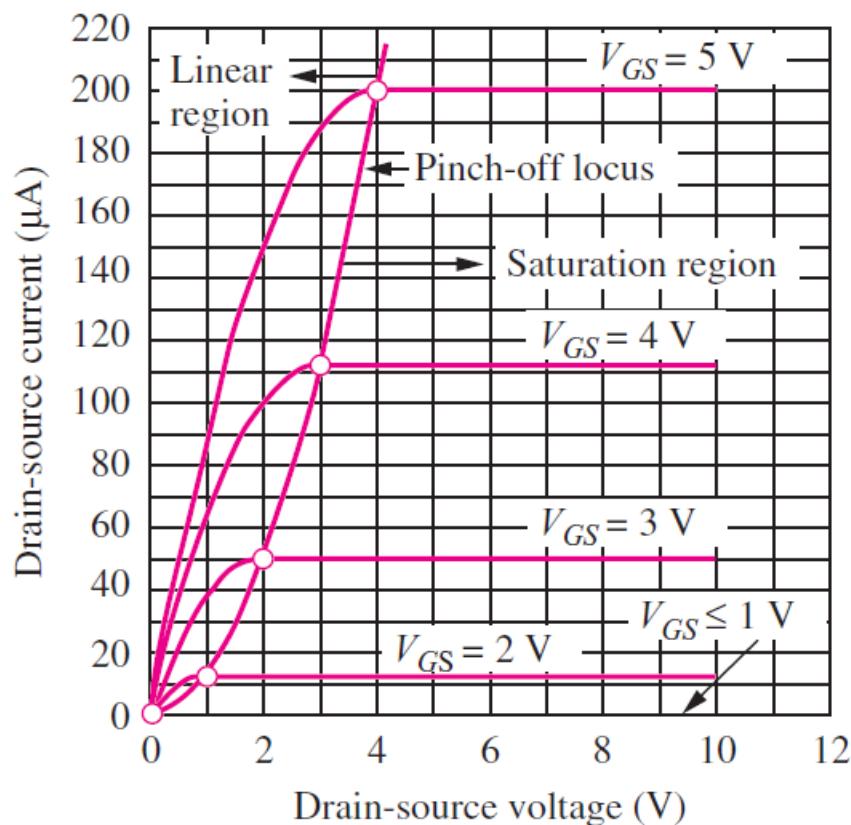


- $v_{DSAT} = v_{GS} - V_{TN}$
- $v_{DS} \geq v_{DSAT}$ :

$$i_D = \frac{K'_n}{2} \frac{W}{L} (v_{GS} - V_{TN})^2$$

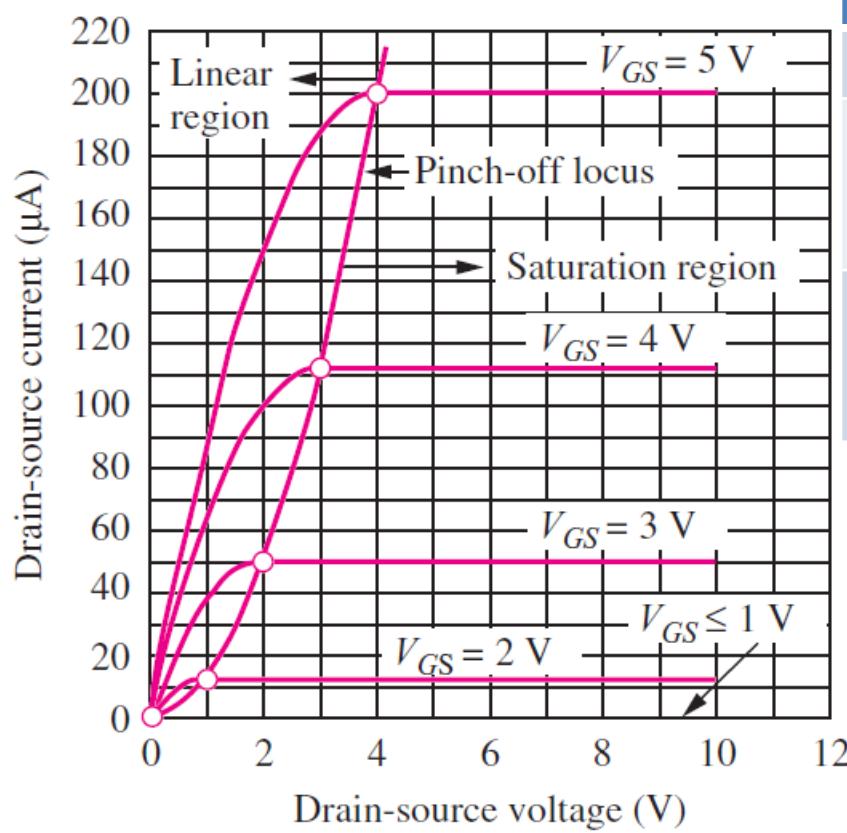


# NMOS Output characteristics



Region	Current Equation	Condition
Cutoff	$i_D = 0$	$v_{GS} \leq V_{TN}$
Triode	$i_D$ $= K_n \left( v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS}$	$v_{GS} > V_{TN}$ $v_{GS} > V_{TN} + v_{DS}$ $[v_{GD} > V_{TN}]$
Saturation	$i_D = \frac{K_n}{2} (v_{GS} - V_{TN})^2$	$v_{GS} > V_{TN}$ $v_{DS} \geq v_{GS} - V_{TN}$

# NMOS Regions and Currents



Region	Current Equation	Condition
Cutoff	$i_D = 0$	$v_{GS} \leq V_{TN}$
Triode	$i_D = K_n \left( v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS}$	$v_{GS} > V_{TN}$ $v_{GS} > V_{TN} + v_{DS}$
Saturation	$i_D = \frac{K_n}{2} (v_{GS} - V_{TN})^2$	$v_{GS} > V_{TN}$ $v_{GS} \leq V_{TN} + v_{DS}$

Example,  $V_{TN}=1V$ :

- $V_{GS}=1V, V_{DS}=1V$ : cutoff
- $V_{GS}=3V, V_{DS}=1V$ : linear
- $V_{GS}=5V, V_{DS}=5V$ : saturation

# Transconductance (Saturation)

---

$$i_D = \frac{K'_n}{2} \frac{W}{L} (v_{GS} - V_{TN})^2$$

- Transconductance (change in  $i_D$  vs. change in  $v_{GS}$ ):

$$g_m = \frac{di_D}{dv_{GS}} = K'_n \frac{W}{L} (v_{GS} - V_{TN})$$

# Transfer characteristics

---

- Fix  $v_{DS}$ , see how  $i_D$  varies with  $v_{GS}$

➤  $v_{GS} < V_{TN}$ , cut-off

$$i_D = 0$$

➤  $V_{TN} \leq v_{GS} \leq V_{DS} + V_{TN}$ , saturation

$$i_D = \frac{K'_n}{2} \frac{W}{L} (\textcolor{red}{v}_{GS} - V_{TN})^2$$

➤  $V_{DS} + V_{TN} < v_{GS}$ , triode

$$i_D = K'_n \frac{W}{L} \left( \textcolor{red}{v}_{GS} - V_{TN} - \frac{V_{DS}}{2} \right) V_{DS}$$

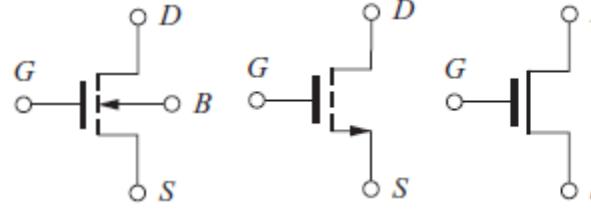
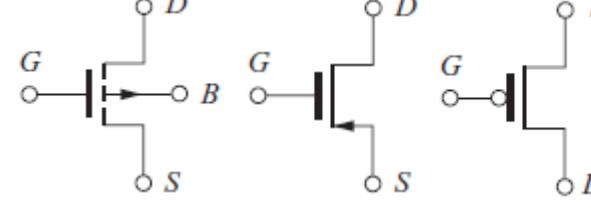
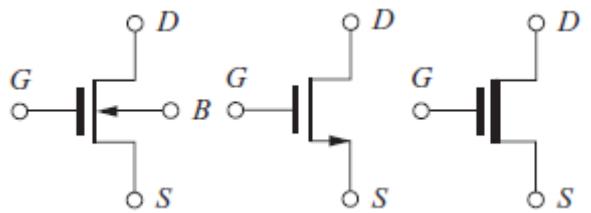
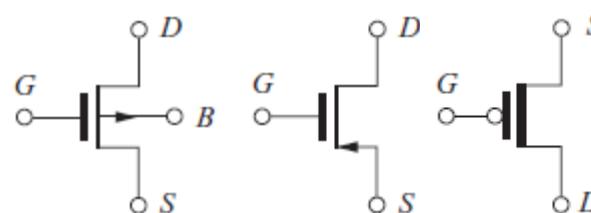
# Transfer characteristics

---

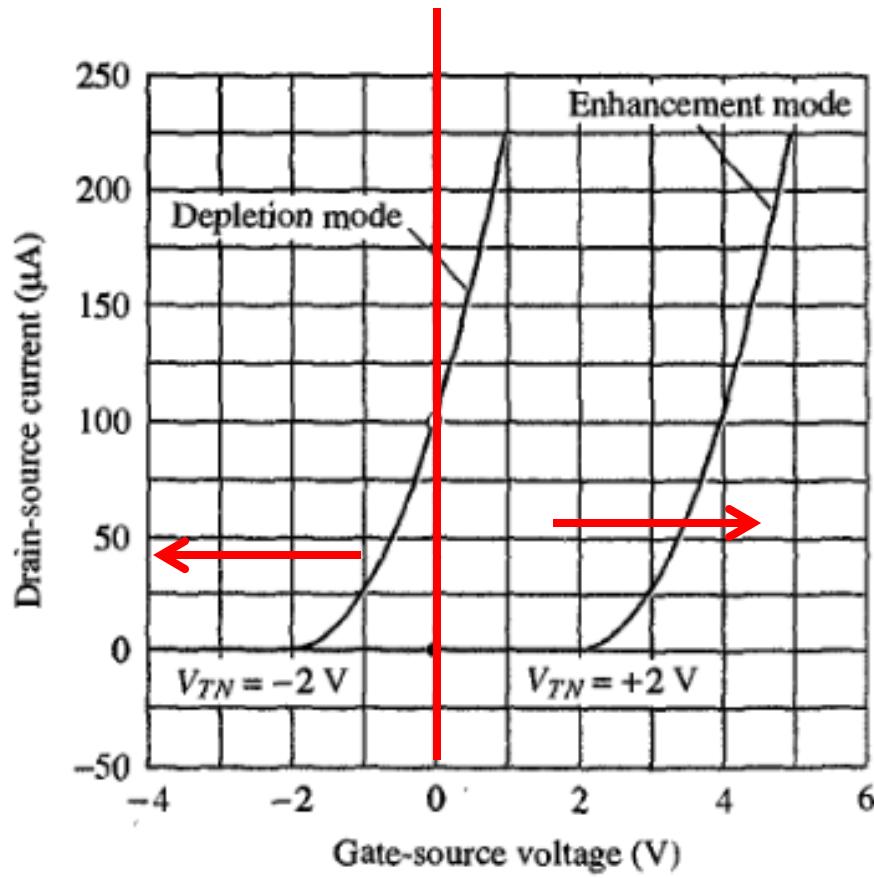
- $i_D$  increases monotonically with  $v_{GS}$  when MOSFET is on ( $v_{GS} > V_{TN}$ ).
- $V_{TN}$  can be either positive or negative.
  - $V_{TN}$  positive, NMOS is OFF for  $v_{GS} = 0 \Rightarrow$  **Enhancement-mode** NMOS transistor (applying positive  $v_{GS}$  **enhances** channel conduction)
  - $V_{TN}$  negative, NMOS is ON for  $v_{GS} = 0 \Rightarrow$  **Depletion-mode** NMOS transistor (applying negative  $v_{GS}$  **depletes** conduction layer)

# MOSFET Circuit Symbols

---

	<b>NMOS</b>	<b>PMOS</b>
<b>E-Mode</b>	 Three NMOS transistors in E-mode. The first two have their drain terminals (D) connected to ground. The third has its drain terminal (D) connected to its source terminal (S). All three have their gate terminals (G) connected to a common signal line. The body terminals (B) are also connected to ground.	 Three PMOS transistors in E-mode. The first two have their drain terminals (D) connected to a power supply. The third has its drain terminal (D) connected to its source terminal (S). All three have their gate terminals (G) connected to a common signal line. The body terminals (B) are also connected to a power supply.
<b>D-Mode</b>	 Three NMOS transistors in D-mode. The first two have their drain terminals (D) connected to a power supply. The third has its drain terminal (D) connected to its source terminal (S). All three have their gate terminals (G) connected to a common signal line. The body terminals (B) are also connected to a power supply.	 Three PMOS transistors in D-mode. The first two have their drain terminals (D) connected to ground. The third has its drain terminal (D) connected to its source terminal (S). All three have their gate terminals (G) connected to a common signal line. The body terminals (B) are also connected to ground.

# Transfer Characteristics



Transfer characteristics for enhancement-mode and depletion-mode NMOS transistors